Test Bench :

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 28.09.2021 21:30:52

// Design Name:

// Module Name: traffic\_light\_tb

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

`define clk\_period 1000000000

module traffic\_light\_tb();

reg clk;

reg rst;

wire [2:0] light\_A;

wire [2:0] light\_B;

traffic\_light TRAFFIC\_LIGHT(

.clk(clk),

.rst(rst),

.light\_A(light\_A),

.light\_B(light\_B)

);

initial clk = 1;

always #(`clk\_period/2) clk = ~clk;

initial begin

rst = 0;

#`clk\_period;

rst = 1;

#`clk\_period;

rst = 0;

#(`clk\_period \* 200);

$stop;

end

endmodule